MANIPAL UNIVERSITY JAIPUR

International Summer School-Manipal University Jaipur [ISSMUJ]-2025

[Offline Mode]

Course Overview

Name of Course- VLSI circuit design using Cadence: From Schematic to Layout

Name of instructor: Dr Neha Singh (Manipal University Jaipur)/ Dr Jyoti Sharma (BIT Mesra, Ranchi, Extension centre Jaipur)

Session: May-July 2025

Language of instruction: English

Number of contact hours: 36

Credit awarded: 03

Prerequisite: Knowledge of digital circuits. Exposure to circuit simulation concepts is added advantage

Objective of Course/Project:

1. To gain practical exposure to the custom VLSI design process
2. To design and simulate a CMOS-based circuit at the schematic level
3. To develop corresponding physical layouts using Cadence Virtuoso
4. To verify the layout using Design Rule Check (DRC) and Layout Versus Schematic (LVS).

Syllabus:

Overview of VLSI design. VLSI Design cycle. CMOS Inverter: Basics, Inverter Transfer characteristics, transistor sizing. Digital circuits: adders and multipliers. Introduction to Cadence Design Environment: design entry using schematic, netlist generation and HSPICE simulation, creating new symbols, generating layout, DRC, creating pins, Layout vs Schematic check.

Organization of Course/Project:

Total contact Hours: 36		
1st week:	10 hrs (classes)	2 hrs (self-study)

2nd week:	10 hrs (hands-on project)	2 hrs (Mid-term assessment/discussion)
3rd week:	10 hrs (hands-on project)	2 hrs (self-study/project)
4th week:	6 hrs (hands-on project)	2hrs (End term exam)

Mode of lectures: Physical and Hands-On Project

Course/Project Plan:

Lecture no.	Topic	Lecture mode	Instructor
L: 1-3	Overview of VLSI design. VLSI Design cycle.	Physical	Dr Neha Singh
L: 4-6	CMOS Inverter: Basics, Inverter Transfer characteristics, transistor sizing.	Physical	Dr Neha Singh
L: 7-10	Digital circuits: adders and multipliers	Physical	Dr Neha Singh
L: 10-11	Introduction to Cadence Design Environment: design entry using schematic,	Physical	Dr Neha Singh
L:12-15	Enter schematic for project: adder and multiplier	Physical	Dr Jyoti Sharma
L:16-17	netlist generation and HSPICE simulation,	Physical	Dr Jyoti Sharma
L: 18-20	creating new symbol, generating layout,	Physical	Dr Jyoti Sharma
L:21-23	DRC and correction	Physical	Dr Jyoti Sharma
L: 24-26	Creating pins, Layout vs Schematic check.	Physical	Dr Jyoti Sharma
L: 27-31	Result compilation and comparison	Physical	Dr Neha Singh
L: 32-36	Paper writing	Physical	Dr Neha Singh

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Brief profile of the instructors:

Dr Neha Singh is a well-rounded and dynamic teaching professional with 20 years of in-depth experience in educating undergraduate and postgraduate engineering students in Electronics & Communication Engineering. She is currently working in the Department of Electronics & Communication Engineering at Manipal University Jaipur, Rajasthan, India. She did her PhD in the year 2020. Her areas of research interest include VLSI design and nanodevices, image Processing, and Machine learning. She has several indexed papers and book chapters published in Journals, conferences and books of repute. She has co-authored engineering textbooks and edited three books with international publishers. She has served as reviewer in various International and peer reviewed Journals and conferences. She has convened various international conferences and other events. She has guided several M Tech Dissertations and B Tech projects and guided PhD scholars as well. She is a Senior Member of IEEE.

Dr. Jyoti Sharma is an Assistant Professor in the Department of Electronics and Communication Engineering at Birla Institute of Technology, Mesra – Jaipur Campus. She holds a Ph.D. in VLSI Design from Malaviya National Institute of Technology (MNIT), Jaipur (2024), an M.Tech. in VLSI Design from MNIT Jaipur (2009), and a B.E. in Electronics and Communication Engineering from the University of Rajasthan (2004). With over 20 years of academic experience, she has served at BIT Mesra Jaipur since 2010, previously holding teaching positions at RCEW Jaipur (2006–2010) and RCERT Jaipur (2004–2006). Her research interests include VLSI Design, Analog and Mixed-Signal Circuit Design, Low Power CMOS Circuits, Nanotechnology in Circuit Design, and Technologies Beyond CMOS. Dr. Sharma has published several papers in reputed journals and conferences such as IEEE, Springer, and Elsevier. She is actively involved in institutional responsibilities, serving as Faculty Coordinator of the Student Alumni Relationship Cell (SARC), a member of the Training & Placement Cell and the Entrepreneurship Cell, and Coordinator of the Internship Committee under the Institution's Innovation Council (IIC). She is a Member of professional bodies like IETE, IEEE. She has also conducted and participated in numerous Faculty Development Programs (FDPs) on VLSI, IoT, and Embedded Systems and holds certifications in Cadence Design Tools, Tanner Tools, and other VLSI platforms.